

**CSE 460**

**VLSI DESIGN**

**Lab Assignment 5**

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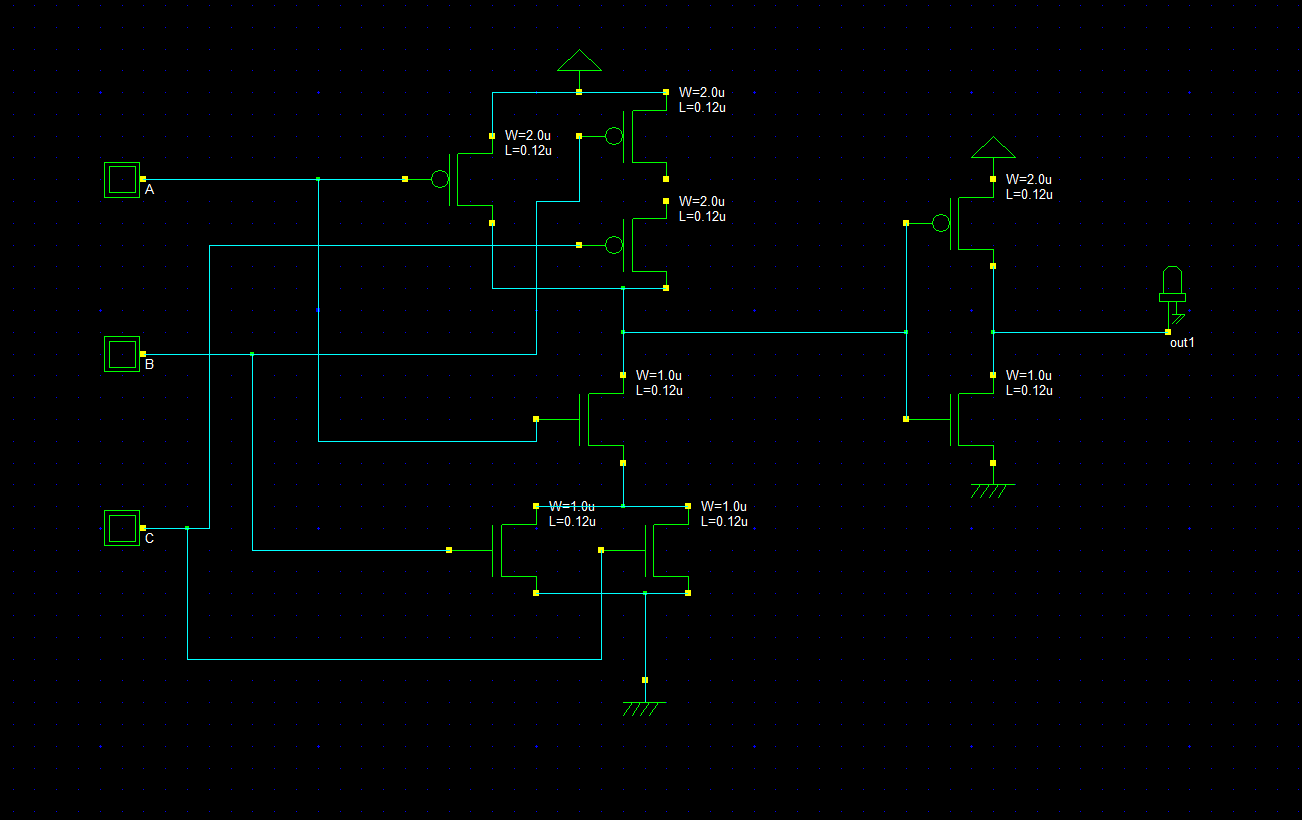
**Sec: 09**

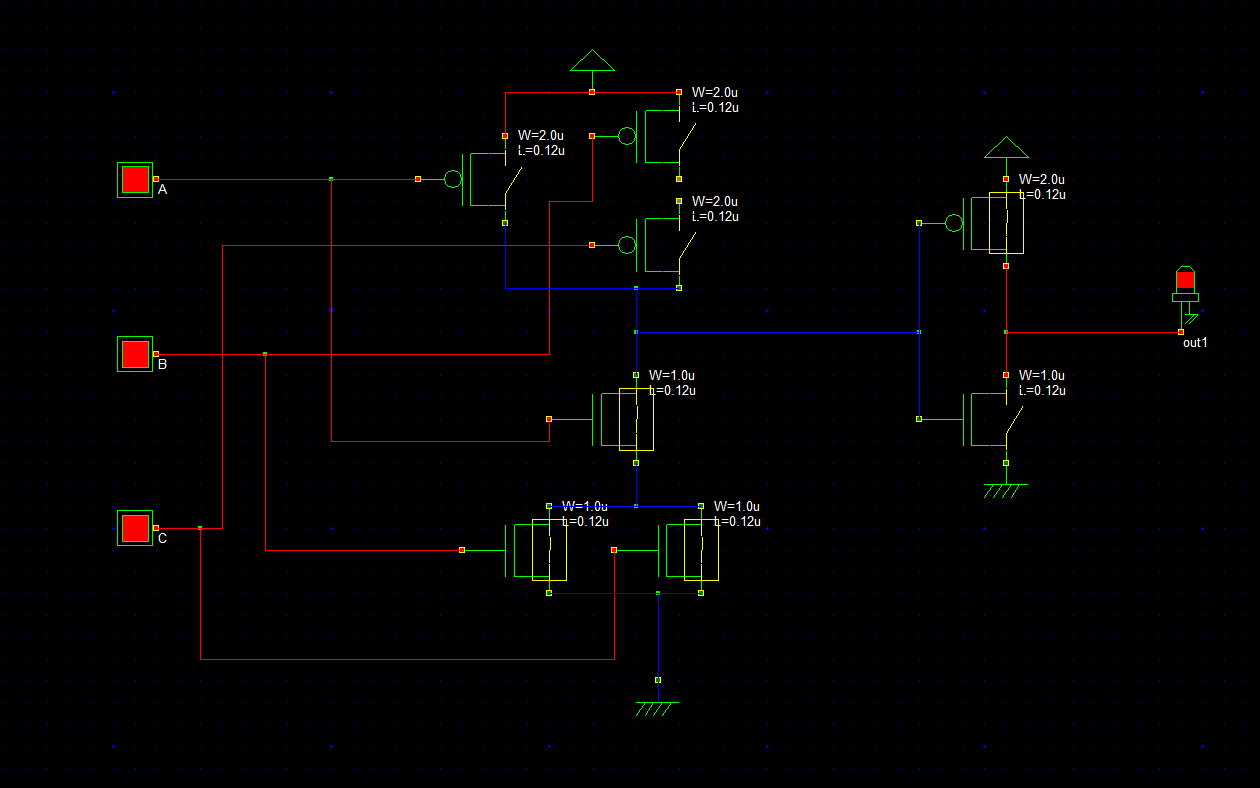
***Problem 1:*** Implement the following Boolean logic expression using CMOS (PMOS+NMOS). Don't use any logic gate directly in your schematic, you have to implement the logic using MOSFETs. F = A(B+C)

**2. Truth Table**

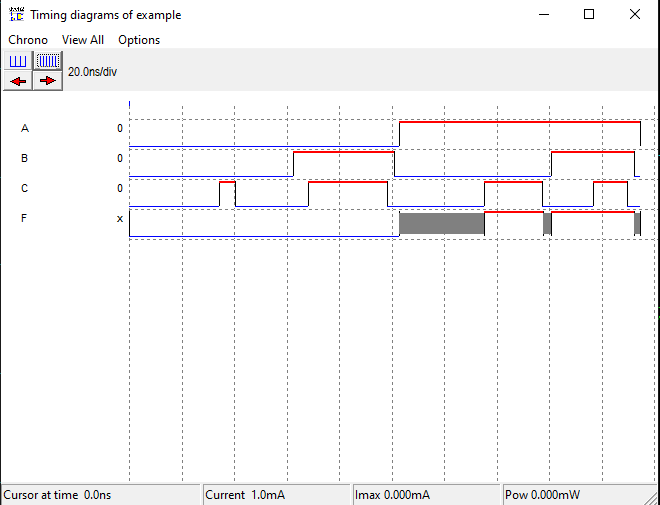
|  |  |  |  |
| --- | --- | --- | --- |
| **a** | **b** | **c** | **f** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** |

**3. Screenshots of schematics**

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**4. Timing Diagram**

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**Explain:**

In this timing diagram, it clearly manifests desired output. From the truth table we can see in this logic function the output is 1 when the input combination A,B,C is 101 , 110, 111 . In the timing diagram we also see the output is 1 when input is 101,110,111 . It matches with the truth table.